

MULTIMEDIA



UNIVERSITY

STUDENT ID NO

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MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2017/2018

**ECE2046 – COMPUTER ORGANIZATION AND
ARCHITECTURE**
(TE/EE/CE/ME/OPE/NANO)

8 MARCH 2018
9:00 a.m – 11:00 a.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 6 pages including cover page with 5 Questions only.
2. Attempt **ALL** Questions. The distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Question 1

- (a) What is Moore's law? State three consequences of this law on the computer industry. [4 marks]
- (b) Explain the meaning of computer organization and computer architecture. [4 marks]
- (c) With the aid of a diagram, illustrate the structure of a computer. [2 marks]
- (d) Draw a diagram and explain the fetch-execute cycle of a computer. [5 marks]
- (e) A main memory has 128 words where each word is 1 byte long and occupies one location in the main memory. Besides that, there are a total of 32 lines in the cache where each line has 8 bytes. Assuming a set associative cache mapping function, answer the following questions:
- (i) Briefly describe how set associative mapping works. [2 marks]
- (ii) Calculate the number of blocks in the main memory. [2 marks]
- (iii) There are 2 bits reserved for the Tag field of the address. Calculate the number of sets that are present in the cache. Consequently, calculate the number of bits reserved for the Word field of the address. [4 marks]
- (iv) Calculate the number of lines in each set of the cache. [2 marks]

Continued...

Question 2

- (a) With the aid of a diagram, explain the types of Queuing scheduling (Queuing representation of processor scheduling) in multiprogramming based operating system.

[6 marks]

- (b) Describe the operating system approach employed in time-sharing systems.

[2 marks]

- (c) With the aid of a diagram, explain the five process states involved in short-term scheduling.

[7 marks]

- (d) Describe the logical address and physical address used in Paging.

[2 marks]

Continued...

Question 3

- (a) Describe the steps to form the negation of an integer in two's complement representation.

[1 mark]

- (b) Perform the following arithmetic operations:

- (i) $-77_{10} + 50_{10}$ using 8-bit two's complement notation.

[2 marks]

- (ii) $1010_2 \times 0101_2$ [Unsigned] using Sequential Multiplication.

[2 marks]

- (c) Using Booth's algorithm, multiply the decimal integers -3 (multiplicand) and -5 (multiplier).

[7 marks]

- (d) Store the following fractional numbers using IEEE single precision floating-point format:

- (i) 79.125_{10}

[2 marks]

- (ii) $1000\ 0010.0111_2$ [12-bit two's complement fixed-point notation]

[3 marks]

Continued...

Question 4

- (a) An address field in an instruction contains decimal value 200. Identify the location for corresponding operand for the following addressing modes:

- (i) Immediate addressing. [1 mark]
- (ii) Direct addressing. [1 mark]
- (iii) Indirect addressing. [2 marks]
- (iv) Register addressing. [1 mark]

- (b) Write an assembly program for a three-address machine to compute:

$$Z = (P \times Q - R) / (S \times T + U)$$

[5 marks]

- (c) In a control unit, the instructions have to be broken down further into micro-operations.

- (i) Describe the term micro-operations. [3 marks]
- (ii) Discuss the different usage of the four internal registers of a microprocessor, including Memory Address Register (MAR), Memory Buffer Register (MBR), Program Counter (PC), and Instruction Register (IR). [6 marks]
- (iii) Write the possible sequence of micro-operations for the opcode **MUL R0, A**. [6 marks]

Continued...

Question 5

- (a) Using a suitable diagram, describe the main difference between pipeline and superpipeline.

[3 marks]

- (b) What is true data dependency?

[2 marks]

- (c) Superscalar architecture has its limitations. State five of these fundamental limitations.

[5 marks]

- (d) Multiprocessing systems can be implemented either by multiprocessors or multicore processors. State three advantages of multicore processors over multiprocessors.

[6 marks]

End of Paper